CLAIMS

1. A semiconductor device characterized in that

connection pads for wire bonding are arranged at peripheral regions of an electrode terminal formation surface of a semiconductor chip,

test pads for testing the semiconductor chip are arranged in an inside region surrounded by said peripheral regions of said electrode terminal formation surface, and

a plurality of rewiring patterns extend from the peripheral regions to said inside region of said electrode terminal formation surface and the individual rewiring patterns connect the individual electrode terminals and the corresponding connection pads and test pads.

2. A semiconductor device as set forth in claim 1, characterized in that the test pads are arranged in an array on said inside region.

3. A semiconductor device as set forth in claim 1 or 2, characterized in that said electrode terminals are exposed from openings of a protective insulation layer covering said electrode terminal formation surface, said rewiring patterns extend on said protective insulation layer and are connected to said electrode terminals via said openings, said rewiring patterns and said protective insulation layer are further covered by an insulation layer, and said connection pads and said test pads connected to said rewiring patterns are exposed from openings of said insulation layer.

4. A semiconductor device comprised of one or a stack of a plurality of the semiconductor device as set forth in any one of claims 1 to 3 as an element semiconductor device or a stack of one or more of each of said element semiconductor device and a semiconductor chip carried on a wiring board, said semiconductor device characterized in that

connection pads of each said element

semiconductor device and connection electrodes of said wiring board are connected by wire bonding, and

each said element semiconductor device and/or each said semiconductor chip is sealed by resin on said wiring board.

5. An interposer characterized in that

connection pads for wire bonding to be connected to a wiring board are arranged at peripheral regions of one surface of the interposer for carrying a semiconductor chip,

test pads for testing the semiconductor chip are arranged in an inside region surrounded by said peripheral regions of said one surface or the other surface, and

a plurality of rewiring patterns extend from said peripheral regions to said inside region and the individual rewiring patterns connect the corresponding connection pads and test pads.

6. An interposer as set forth in claim 5, characterized in that said test pads are arranged in an array in said inside region.

7. A semiconductor device comprised of a semiconductor module, comprised of an interposer as set forth in claim 5 or 6, on the surface of which opposite to the surface where said test pads are arranged, one or a plurality of said semiconductor chips are stacked, carried on a wiring board,

said semiconductor device characterized in that

connection pads of said interposer and connection electrodes of said wiring board are connected by wire bonding, and

said semiconductor module is sealed by resin on said wiring board.

8. A semiconductor device as set forth in claim 7, characterized in that a semiconductor module where a surface where said test pads are formed is exposed and a

semiconductor chip carrying surface of the interposer is sealed by a resin.